Arasan Chip Systems Introduces First eMMC v5.0 I/O PADs & PHY IP using TSMC 28nmHPM Process

Arasan's Total IP Solution for newly released eMMC v5.0 Mobile Storage Standard Provides Quick Path to Silicon Success. See product demo at ARM TechCon.

San Jose, California – October 28, 2013 - Arasan Chip Systems, Inc. ("Arasan"), a leading provider of Total IP Solutions for mobile applications announced today the availability of the most complete solution for the latest eMMC standard: Embedded MultiMediaCard (eMMC), Electrical Standard (5.0). Arasan's eMMC v5.0 Total IP Solution includes eMMC 5.0 host and device IP, software stack and driver, verification IP and now the analog PHY and PAD set required for use in today's embedded mobile storage for smart phones and tablets. Arasan's new eMMC v5.0 solution uses TSMC's 28HPM process to address the need for applications requiring high speed as well as low leakage power.

The Arasan PAD set fully supports the eMMC 5.0 HS400 specification at 3.3v output. At 200 MHz, the required clock speed of HS400, a DLL is required to ensure accurate data transfer. The HS400 mode uses a 200 MHz clock and DDR signaling to achieve a maximum bandwidth of 400 MB/s. The Arasan eMMC PHY IP includes an analog PHY comprising three DLLs needed for tuning, strobe and hold time management.

Visit the Arasan booth at ARM TechCon on Wednesday, October 30, from 10am-7:15pm and Thursday, October 31, from 10am-4pm, at the Santa Clara Convention Center, Santa Clara, California, Booth #609 for a demonstration of the new Arasan eMMC v5.0 Total IP Solution.

"Arasan is the market leader in analog and digital IP for mobile storage. By making these ready-to-use PADs and PHY available, eMMC 5.0 implementation is simplified, especially for teams without analog layout skills," said Andrew Haines, VP of worldwide marketing at Arasan. "Our 28nm eMMC solution represents the latest result of Arasan's on-going investment in analog and digital Total IP Solutions for JEDEC, SD Association, MIPI and USB standards."

Last month JEDEC published the latest version of the eMMC v5.0 standard that defines new functionalities and enhancements for embedded mass-storage flash memory widely used in consumer electronics, including tablets, smartphones, GPS systems, eReaders and other mobile computing devices. The previous version of the standard that supported speeds up to 200 Mega Transfers per Second permitted a digital implementation. eMMC v5.0 doubles the bandwidth to 400MB/s, but requires analog components (I/O PADs and PHY). At this performance level, interface timing tuning, which has been a feature of eMMC, must be done in an analog PHY instead of using a simple tapped delay line.

eMMC is an embedded non-volatile memory system, consisting of both flash memory and a flash memory controller that simplifies the application interface design and frees the host processor from low-level flash memory management. This benefits product developers by reducing time-to-market as well as facilitating support for future flash device offerings. eMMC, offered in small BGA package sizes featuring low power consumption, is the dominant, low-cost memory solution for mobile and other space-constrained products.

Arasan's 28nm eMMC 5.0 PHY consists of three components

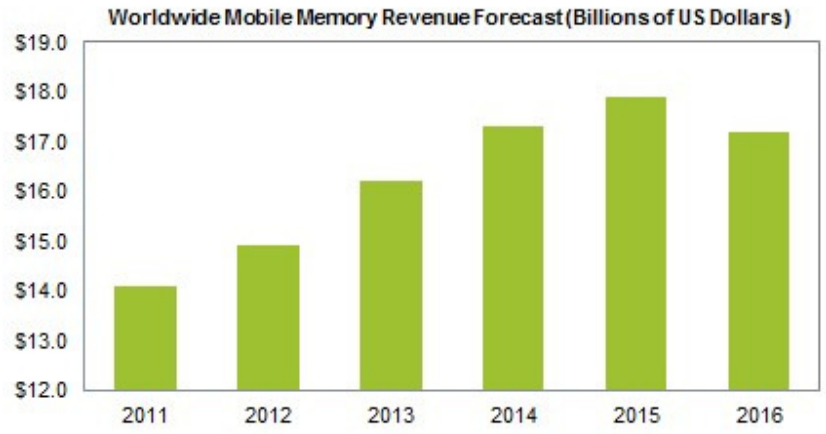
First, Arasan's 28nm general purpose I/O PADs are multipurpose PADs that can be programmed to operate in different modes: 1) Output with predetermined source/sink impedance, 2) Open drain, 3) Input, 4) Tristate and 5) Weak pull up or pull down. The I/O PADs are specially designed to seamlessly integrate with Arasan's eMMC 5.0 host controller IP.

The PAD is designed using TSMC's 28HPM process technology. With such wide performance/leakage coverage, the 28HPM process is ideal for many applications from networking, tablets, to mobile consumer products.

Second, the Arasan DLL works in conjunction with a 32 tap delay line and multiplexing logic to align the placement of clock edges. It utilizes the 28nmHPM process and is intended for core voltage of 0.9V and I/O voltage of 3.3V.

Third, the Arasan solution provides a calibration I/O PAD that automatically goes to a low power state after resistor value selection. This architecture minimizes power and area in a design.

About eMMC
eMMC is the dominant flash interface in cell phones and tablets today. Shipments of eMMC solutions this year are forecasted to reach 700 million according to an IHS iSuppli Mobile & Embedded Memory Market Tracker report in segments such as tablets, e-book readers and portable GPS navigation devices. The eMMC v5.0 standard is projected to ramp quickly in mainstream devices. By 2015, mobile memory revenue will peak at $17.9 billion (see chart).



Source: IHS iSuppli Research, May 2012

Availability
Arasan's 28nm eMMC v5.0 PAD and PHY offering is available now.

About Arasan
Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers, and optional customization services for MIPI, USB, UFS, SD, SDIO, MMC/eMMC, UFS, and many other popular standards. Arasan's Total IP products serve system architects and chip design teams in mobile,

gaming and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Unlike many other IP providers, Arasan's Total IP Solution encompasses all aspects of IP development and integration, including analog and digital cores, hardware development kits, protocol analyzers, validation IP and software stacks and drivers and optional architecture consulting and customization services. Based in San Jose, CA, USA, Arasan Chip Systems has a 17 year track record of IP and IP standards development leadership.

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