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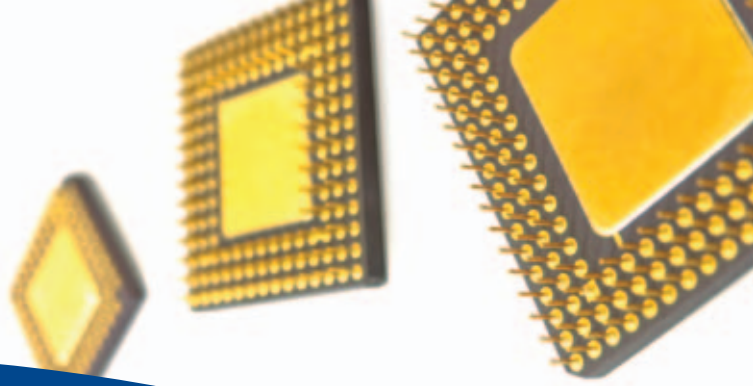


eSi-RISC

eSi-1600 – 16-bit, low-cost & low-power CPU

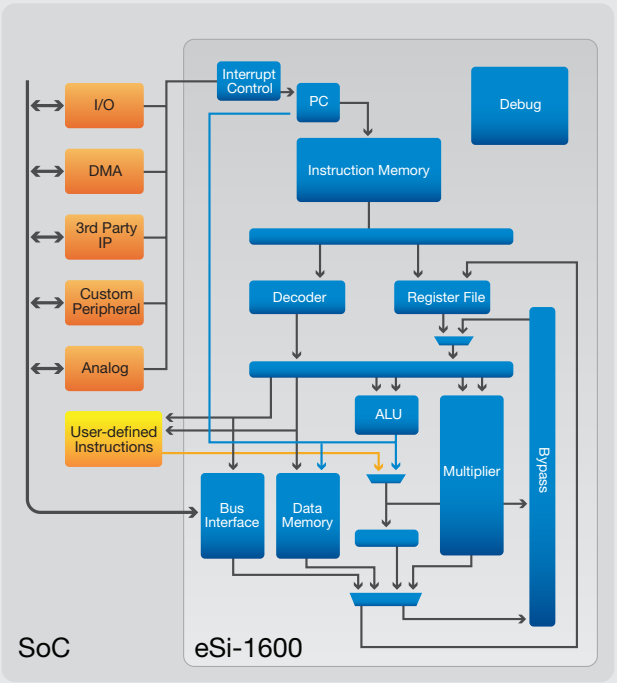
EnSilica's eSi-1600 CPU IP core is an extremely small, low-cost and low-power processor ideal for integration into ASIC and/or FPGA designs. It offers similar performance to more expensive 32-bit CPUs, while having a system cost comparable to that of 8-bit CPUs. Significant power savings are possible compared to 8-bit CPUs as applications require far fewer clock cycles to run.

Features

- 16-bit RISC architecture
- 16 general purpose registers
- 92 basic instructions and 10 addressing modes
- Supports up to 90 user-defined instructions
- 5-stage pipeline
- Harvard or von Neumann memory architecture
- AMBA AHB and APB peripheral bus
- Optional support for user and supervisor modes
- Up to 16 interrupts plus NMI and system call
- Fast interrupt response time of 6-9 cycles
- JTAG or serial debug
- Up to 0.7 DMIPS per MHz
- High code density
- ASIC performance (Typical 0.13um):
  - Up to 600 MHz
  - From 8.5k gates
  - From 15uW/MHz
- FPGA Performance (Virtex 5):
  - Up to 160 MHz
  - From 1100 LUTs
- High quality IP:
  - Verilog RTL
  - DFT ready
  - Silicon proven
- C and C++ software development using license-free toolchain, under industry standard Eclipse IDE
- Easy migration path to 32-bit version

Applications

- Home automation
- Industrial control
- Medical
- Low-power wireless
- Data communication
- Power management



Architecture

The eSi-1600 16-bit CPU is the smallest member in the eSi-RISC family of processor cores from EnSilica. It is targeted specifically for low-cost and low-power applications, where typically an 8-bit CPU may have previously been used, or where a 32-bit CPU is too big or power hungry.

Even though it is 16-bit, the gate count is equivalent to many 8-bit cores due to the simplicity of the RISC pipeline. With a wider datapath and 16 general purpose registers, application programs are able to execute in far fewer clock cycles. This can save a significant amount of power by either allowing the CPU to be clocked at a lower frequency or by being able to enter a power down state sooner.

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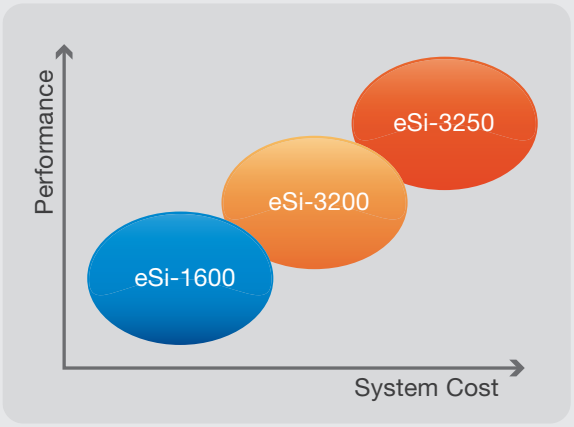
For applications where high performance is required, the 5-stage pipeline allows extremely high clock frequencies to be achieved. The optimising C/C++ compiler is fully aware of the pipeline and is able to schedule instructions to eliminate latencies. Static branch prediction is employed to minimize the cost of branch instructions.

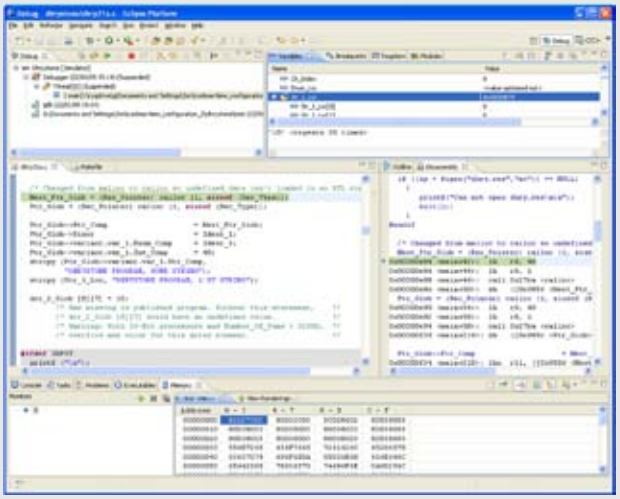
The eSi-1600's instruction set includes arithmetic and logical instructions (including barrel-shift, multiply and divide), comparisons, load and stores, branches and calls as well as system level instructions to control interrupts and enter lower power states. There are also a number of optional instructions and addressing modes that can be selected, should a specific application require them. For those applications that require extreme performance or ultra low power, user-defined instructions and registers can be implemented.

Hardware debug facilities include hardware breakpoints, watchpoints, null pointer detection and single-stepping for fast debugging of ROM, FLASH and RAM based programs.

Scalability

For applications that require even more performance or require more memory than is catered for by the eSi-1600, the eSi-32xx range of 32-bit processors are available. These processors feature the same ISA as the eSi-1600, extended to 32-bits. The processors RTL and toolchain share a common code base, resulting in an easy migration path for both software and hardware developers, should the demands of an application change.





Eclipse Integrated Development Environment

Toolchain

The toolchain for the eSi-1600 is based upon the industry standard GNU toolchain, which includes an optimising C and C++ compiler, assembler, linker, debugger, simulator and binary utilities. All these tools can be driven by the customizable Eclipse IDE. The debugger can connect to the target CPU either via JTAG, a serial interface or the Verilog PLI.

Complete C and C++ libraries are supplied. Ports of Micrium's uC/OS-II RTOS, FreeRTOS and the lwIP TCP/IP stack are available. The toolchain is available for both Windows and Linux hosts and is available to use at no cost.

IP Delivery

The eSi-1600 is delivered as a Verilog RTL IP core. The design is target technology independent, although alternative implementations of some modules are available, such as the multiplier and JTAG interface, which are specifically optimised for FPGAs. The design is DFT ready, supporting full scan insertion for all flip flops and memory BIST. Example scripts are provided for popular EDA tools.

A selection of AMBA peripherals are supplied with the core, including: UART, SPI, I2C™, Timer, PWM, Watchdog, GPIO, PS/2 and Ethernet MAC. By using an industry standard bus, a wide range of 3rd party IP cores are compatible with the eSi-1600.

About EnSilica

EnSilica is an established company with many years' experience providing high quality front-end IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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