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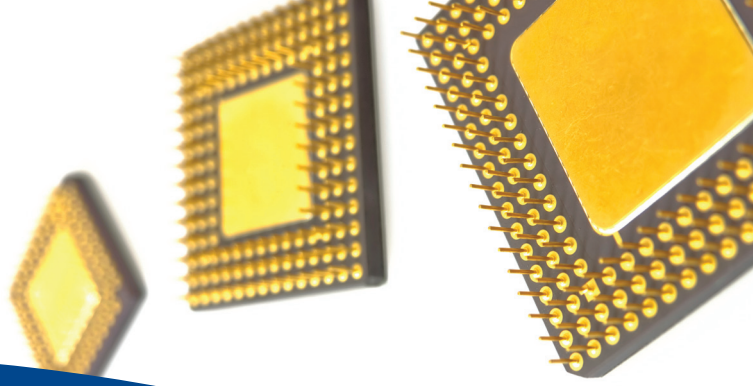


eSi-3200 – 32-bit, low-cost & low-power CPU

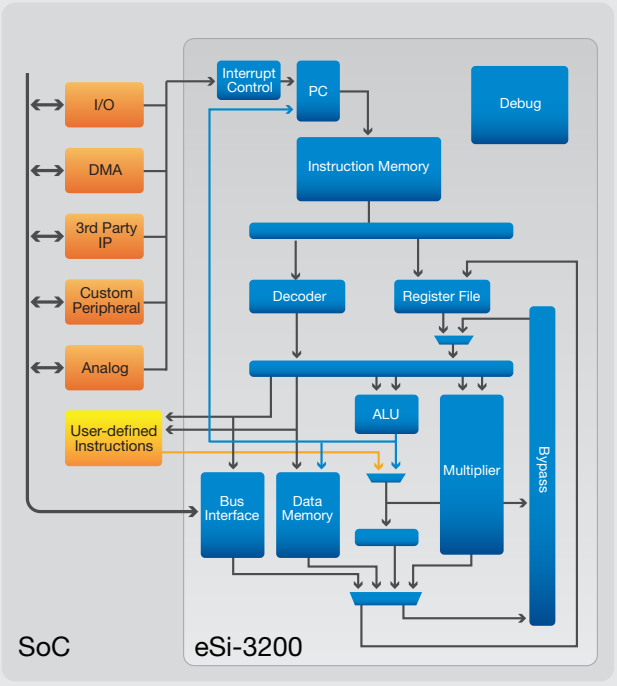
EnSilica's eSi-3200 CPU IP core is an extremely small, low-cost and low-power processor ideal for integration into ASIC and/or FPGA designs with on-chip memories. The eSi-3200 is particularly suited to embedded control applications.

Features

- 32-bit RISC architecture
- 16 or 32 general purpose registers
- 104 basic instructions and 10 addressing modes
- Supports up to 90 user-defined instructions
- 5-stage pipeline
- Harvard or von Neumann memory architecture
- Optional memory protection unit (MPU)
- AMBA AXI or AHB data bus and APB peripheral bus
- Optional support for user and supervisor modes
- Up to 32 interrupts plus NMI and system call
- Fast interrupt response time of 6-9 cycles
- JTAG or serial debug
- Up to 1.41 DMIPS per MHz
- Intermixed 16 and 32-bit instructions result in exceptional code density without compromising performance
- ASIC performance (Typical 90nm):
  - Up to 700 MHz
  - From 15k gates
  - From 18uW/MHz
- FPGA Performance (Stratix IV):
  - Up to 200 MHz
  - From 1800 ALUTs
- High quality IP:
  - Verilog RTL
  - DFT ready
  - Silicon proven
- C and C++ software development using license-free toolchain, under industry standard Eclipse IDE
- Easy migration path to 16-bit version or 32-bit version with caches

Applications

- Consumer
- Industrial control
- Medical
- Communications
- Storage
- Intelligent sensors



Architecture

The eSi-3200 32-bit CPU is the mid-range member in the eSi-RISC family of processor cores from EnSilica. It is targeted specifically for low-cost and low-power applications that require more computational power or a larger address space than is provided by the 16-bit eSi-1600 and that are able to be implemented using on-chip memory. The cacheless memory architecture of the eSi-3200 allows for deterministic performance, making it particularly suitable for hard real-time control applications.

For applications where high performance is required, the 5-stage pipeline allows extremely high clock frequencies to be achieved. Static branch prediction is employed to minimize the cost of branch instructions.

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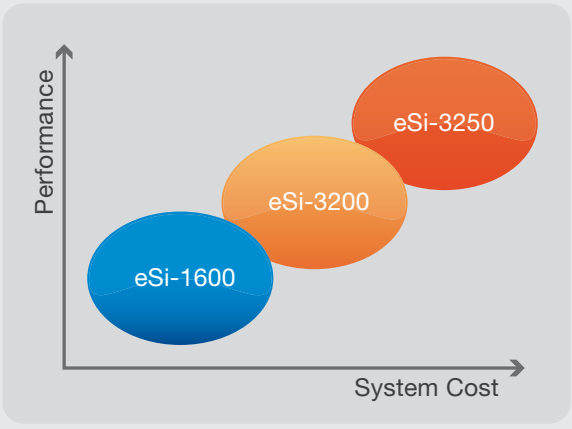
The eSi-3200's instruction set includes arithmetic and logical instructions (including barrel-shift, multiply and divide), comparisons, load and stores, branches and calls as well as system level instructions to control interrupts and enter low power states. There are also a number of optional instructions and addressing modes that can be selected, should a specific application require them. For those applications that require extreme performance or ultra low power, user-defined instructions and registers can be implemented.

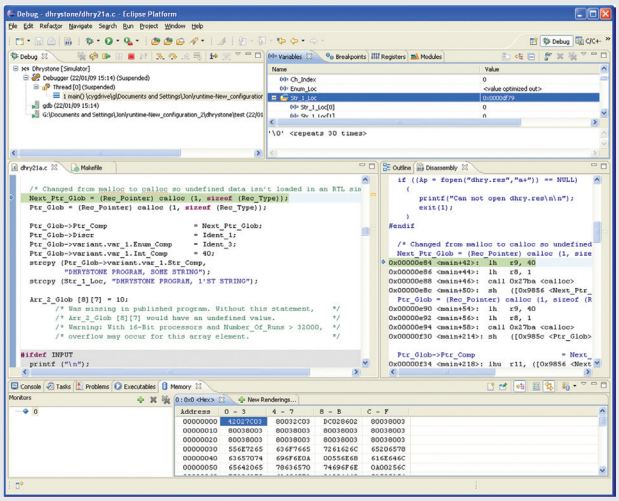
Instructions are encoded in either 16 or 32-bits, depending upon the size of the operands and the type of instruction. All of the commonly used instructions can be encoded in 16-bits. This ensures that high code density is achieved, while minimizing memory accesses to help conserve power.

Hardware debug facilities include hardware breakpoints, watchpoints, null pointer detection and single-stepping for fast debugging of ROM, FLASH and RAM based programs.

Scalability

For applications that require do not require 32-bit performance or more than 64kB of memory, the eSi-1600 16-bit processor can be used. This processor features the same ISA as the eSi-3200, reduced to 16-bits. For 32-bit applications requiring cachable off-chip memory, the eSi-3250 processor can be used. All of the eSi-RISC processors RTL and toolchains share a common code base, resulting in an easy migration path for both software and hardware developers, should the demands of an application change.





Eclipse Integrated Development Environment

Toolchain

The toolchain for the eSi-3200 is based upon the industry standard GNU toolchain, which includes an optimising C and C++ compiler, assembler, linker, debugger, simulator and binary utilities. All these tools can be driven by the customizable Eclipse IDE. The debugger can connect to the target CPU either via JTAG, a serial interface or the Verilog PLI.

Complete C and C++ libraries are supplied. Ports of Micrium's uC/OS-II RTOS, FreeRTOS and the lwIP TCP/IP stack are available. The toolchain is available for both Windows and Linux hosts and is available to use at no cost.

IP Delivery

The eSi-3200 is delivered as a Verilog RTL IP core. The design is target technology independent, although alternative implementations of some modules are available, such as the multiplier and JTAG interface, which are specifically optimised for FPGAs. The design is DFT ready, supporting full scan insertion for all flip flops and memory BIST. Example scripts are provided for popular EDA tools.

A selection of AMBA AHB and APB peripherals are supplied, including: UART, SPI, I²C™, Timer, Watchdog, GPIO, DMA, PS/2 and an Ethernet MAC. By using an industry standard bus, a wide range of 3rd party IP cores are compatible with the eSi-3200.

About EnSilica

EnSilica is an established company with many years' experience providing high quality front-end IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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