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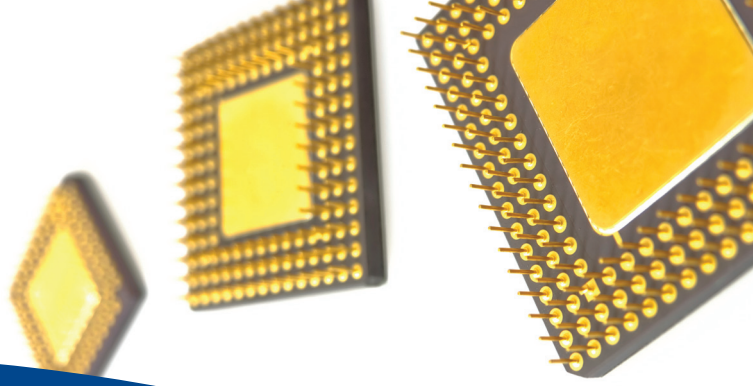


eSi-3250 – 32-bit, high-performance CPU

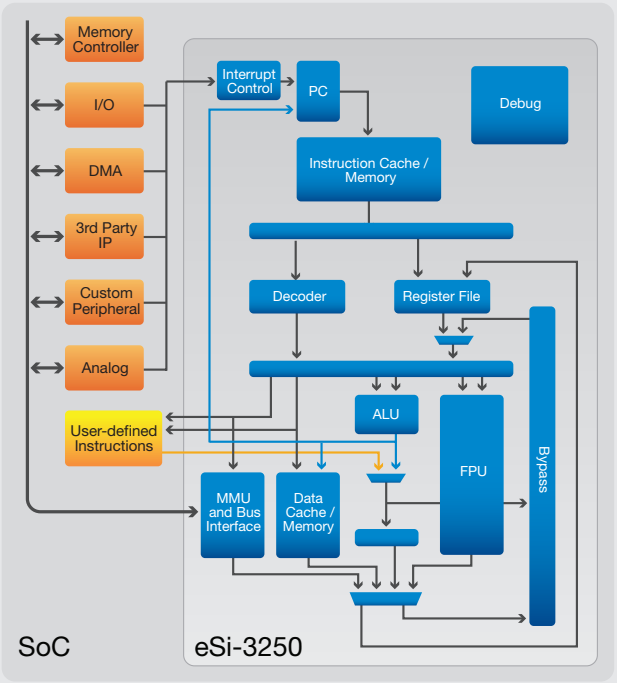
EnSilica's eSi-3250 CPU IP core is a high-performance processor ideal for integration into ASIC and/or FPGA designs with off-chip memories. The eSi-3250 is suited to a wide range of applications including running complex operating systems such as Linux.

Features

- 32-bit RISC architecture
- 32 general purpose registers
- 104 basic instructions and 10 addressing modes
- Optional IEEE 754 floating point unit (FPU)
- Supports up to 90 user-defined instructions
- 5-stage pipeline
- Optional memory management unit (MMU)
- Configurable instruction and data caches (1-64kB, direct mapped or 2 or 4 way associative)
- AMBA AXI or AHB data bus and APB peripheral bus
- User and supervisor modes
- Up to 32 interrupts plus NMI and system call
- Fast interrupt response time of 6-9 cycles
- JTAG or serial debug
- Up to 1.41 DMIPS per MHz
- Intermixed 16 and 32-bit instructions result in exceptional code density without compromising performance
- ASIC performance (Typical 90nm):
  - Up to 700 MHz
  - From 20k gates
  - From 22uW/MHz
- FPGA Performance (Stratix IV):
  - Up to 200 MHz
  - From 2200 ALUTs
- High quality IP:
  - Verilog RTL
  - DFT ready
  - Silicon proven
- C and C++ software development using license-free toolchain, under industry standard Eclipse IDE
- Easy migration path to cacheless version

Applications

- Consumer
- Industrial control
- Medical
- Communications
- General purpose



Architecture

The eSi-3250 32-bit CPU is the top-of-the-range member in the eSi-RISC family of processor cores from EnSilica. It is targeted specifically for applications with high performance and large memory requirements.

The processor features separate instruction and data caches that can be configured in size (from 1- 64kB) and associativity (direct mapped, 2 or 4-way associative) to increase performance when accessing off-chip memory. The optional paged memory management unit (MMU) enables the implementation of virtual memory and the ability to run operating systems such as Linux.

The 5-stage pipeline allows extremely high clock frequencies to be achieved. Static branch prediction is employed to minimize the cost of branch instructions.

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The eSi-3250's instruction set includes everything you would expect in a high-performance processor. There are also a number of optional application specific instructions and addressing modes. For example, a set of IEEE-754 compliant single-precision floating point instructions are available. For those applications that require extreme performance or ultra low power operation, user-defined instructions and registers can be implemented.

Instructions are encoded in either 16 or 32-bits, with all of the commonly used instructions being encoded in 16-bits, maximizing code density and improving cache performance.

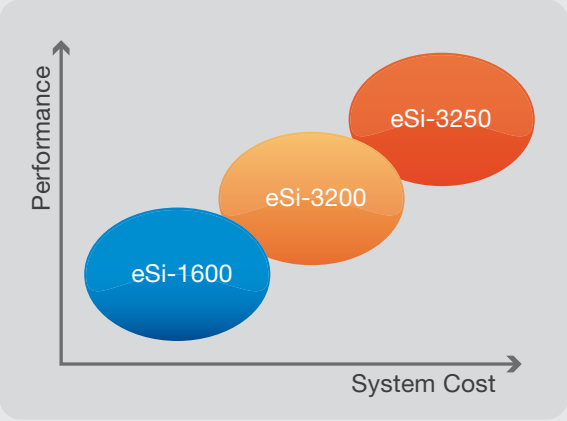
The processor supports both user and supervisor operating modes, with privileged instructions and memory areas, to allow an O/S kernel to be fully protected from user applications.

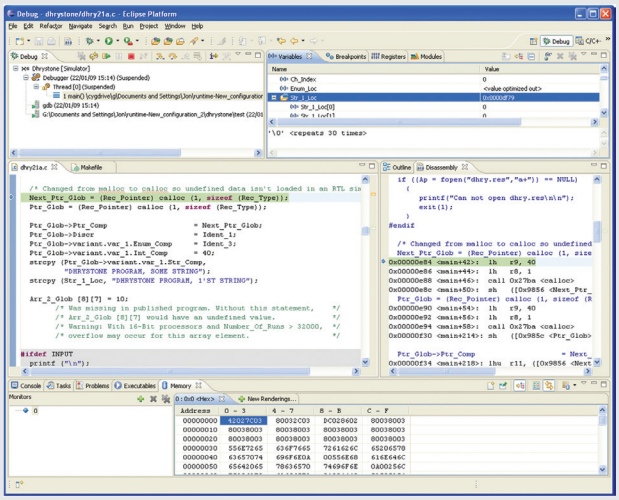
Hardware debug facilities include hardware breakpoints, watchpoints, null pointer detection and single-stepping for fast debugging of ROM, FLASH and RAM based programs.

Scalability

For applications that require do not require off-chip memory, the smaller eSi-3200 is available. For even simpler applications that do not require 32-bit performance or more than 64kB of memory, the eSi-1600 16-bit processor can be used.

All of the eSi-RISC processors RTL and toolchains share a common code base, resulting in an easy migration path for both software and hardware developers, should the demands of an application change.





Eclipse Integrated Development Environment

Toolchain

The toolchain for the eSi-3250 is based upon the industry standard GNU toolchain, which includes an optimising C and C++ compiler, assembler, linker, debugger, simulator and binary utilities. All these tools can be driven by the customizable Eclipse IDE. The debugger can connect to the target CPU either via JTAG, a serial interface or the Verilog PLI.

Complete C and C++ libraries are supplied. Ports of Micrium's uC/OS-II RTOS, FreeRTOS and the lwIP TCP/IP stack are available. The toolchain is available for both Windows and Linux hosts and is available to use at no cost.

IP Delivery

The eSi-3250 is delivered as a Verilog RTL IP core. The design is target technology independent, although alternative implementations of some modules are available, such as the multiplier and JTAG interface, which are specifically optimised for FPGAs. The design is DFT ready, supporting full scan insertion for all flip flops and memory BIST. Example scripts are provided for popular EDA tools.

A selection of AMBA AHB and APB peripherals are supplied, including: UART, SPI, I²C™, Timer, Watchdog, GPIO, DMA, PS/2 and an Ethernet MAC. By using an industry standard bus, a wide range of 3rd party IP cores are compatible with the eSi-3250.

About EnSilica

EnSilica is an established company with many years' experience providing high quality front-end IC design services to customers undertaking FPGA and ASIC designs. We have an impressive record of success working across many market segments with particular expertise in multimedia and communication applications. Our customers range from start-ups to blue-chip companies. EnSilica also offer a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC and the eSi-Comms range of communications IP.

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