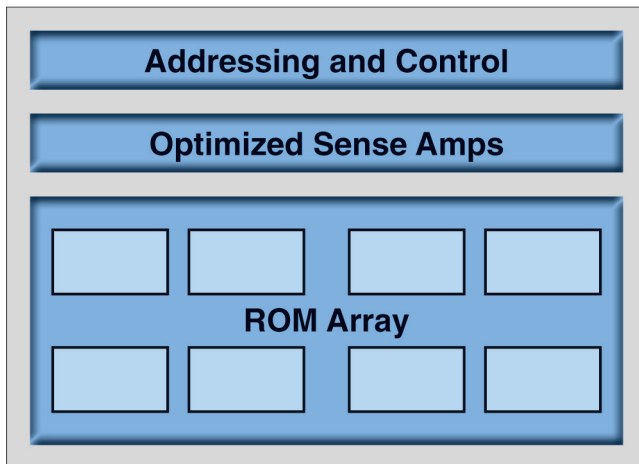


The Novelics compiler-based family of advanced embedded memories includes low-power, high-speed, and high-density configurable coolROM targeting the most demanding applications.

The Novelics coolROM embedded memory IP is the industry's highest density single-layer metal programmable ROM, with a macro size comparable to diffusion-ROM technology. This is achieved with a Novelics proprietary bitcell design that requires fewer transistor contacts per cell than conventional designs. A significantly smaller macro size and reduced capacitance results in significant dynamic power dissipation savings.

The Novelics coolROM is designed specifically with low-leakage applications in mind. The entire ROM core array is automatically maintained with no voltage bias when not in use, resulting in zero ROM core leakage. Peripheral circuits utilize positive channel length bias to further reduce leakage.

A high performance cycle frequency is obtained with advanced decoding and sensing circuits. In addition to fast access time, all control and address inputs require near-zero input setup time for the most demanding high speed applications.



coolROM general architecture

FEATURES:

- Customer architected through the MemQuest memory compiler and characterization tool
- Highest density metal-programmable ROM
- Based on patent pending proprietary high-density, low power cell and system circuitry
- Reliable, silicon-proven architecture
- Single-layer metal 1 programmable
- Uses only up to metal 4-Selectable power, speed, and area
- Selectable word width, depth and aspect ratio
- Comprehensive leakage power management
- Instance size up to 1Mb
- Lowest active power in the industry by more than 5x
- Advanced power management circuits
- Supports a wide range of clock duty cycles
- Near zero set-up time
- Flexible routing over macro in M5 and above

BENEFITS:

- Lower cost due to higher density and standard logic processing
- Ideal for applications requiring ultra-low power at high densities and high-speed applications that can benefit from advanced power management features
- Silicon and production-validation provides manufacturability assurance

MemQuest Memory Compiler

The Novelics MemQuest™ memory compiler is a tool unlike anything that has been available in the chip design world before. MemQuest is a WEB based on-line tool suite that enables the SoC designer to specify and implement CUSTOM memories in a matter of minutes.

Customer Memory Specifications

The chip designer begins the process by entering the specification for the memory that is needed in the design. All of the specification parameters that may drive the implementation of any memory are entered into MemQuest in pull-down menu form.

Architecture trade-off analysis

As each memory is specified, a variety of instance solutions are displayed to the designer. Each axis of performance is represented with a column in the MemQuest output table. With this table, the architecture is evaluated and the design options are traded off based on the requirements for the instance (e.g., area, power, access time, leakage current) and various operating conditions (i.e., PVT = process, voltage, and temperature). Many variables such as wider combinations of muxing and banking can be expanded. Using the MemQuest flow instances can be optimized to align exactly with their required characteristics in the chip.

Selection	Area (mm ²)	X (mm)	Y (mm)	Access Time (ns)	Power (mW)	Active Leakage (mA)	Sleep Leakage (mA)
Operating Conditions (PVT):				wc *	tc	tc	tc
1	0.0039	0.147	0.0265	2.47	0.0029	0.0007	0.0004
2	0.0040	0.0847	0.0472	2.45	0.0023	0.0008	0.0005
3	0.0044	0.147	0.0301	2.43	0.0029	0.0011	0.0005
4	0.0046	0.0847	0.0544	2.42	0.0023	0.0013	0.0007
5	0.0047	0.0535	0.0887	2.59	0.0022	0.001	0.0007
6	0.0055	0.147	0.0373	2.42	0.003	0.0019	0.0007
7	0.0055	0.0535	0.103	2.58	0.0023	0.0017	0.0011
8	0.0058	0.0847	0.0688	2.42	0.0024	0.0023	0.0011
9	0.0065	0.0379	0.172	3.03	0.0026	0.0014	0.0011

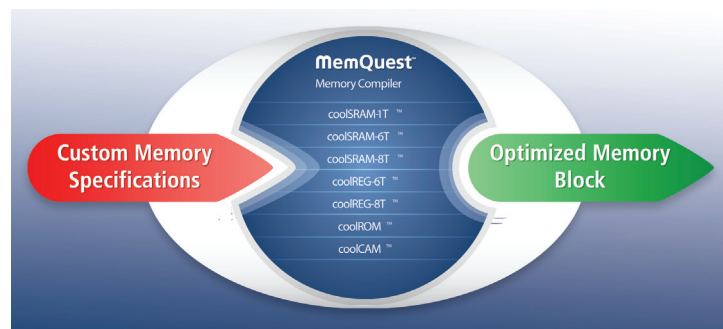
Memory implementation

Once the specification has been completed and the architectural tradeoffs have been chosen, MemQuest immediately generates all of the views and models needed to instantiate the memory in the chip design for simulation. Additionally, the design is submitted to the Novelics on-line servers for physical implementation. A completely automated and correct by construction flow generates the physical implementation of the memory.

Memory verification

Following the automated implementation of the GDS2 for the memory instance, an additional automated program extracts the physical circuit characteristics from the GDS2 models. The program then executes a spice simulation of the exact circuit. In parallel to the automated extraction and characterization flows, another automated sequence of behind the scenes programs is run to verify the physical designs. Complete LVS and DRC verifications are run on each memory as part of this process.

Because each instance is actually characterized and verified by the on-line tools, many more degrees of freedom are available for specification by the designer who uses MemQuest. Using this flow, memories can be characterized at any number of custom corners.



MemQuest is the world's first WEB based on-line CUSTOM memory development tool suite – not merely a narrowly characterized instance generator.

For the latest product information, call us or visit: www.mentor.com

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