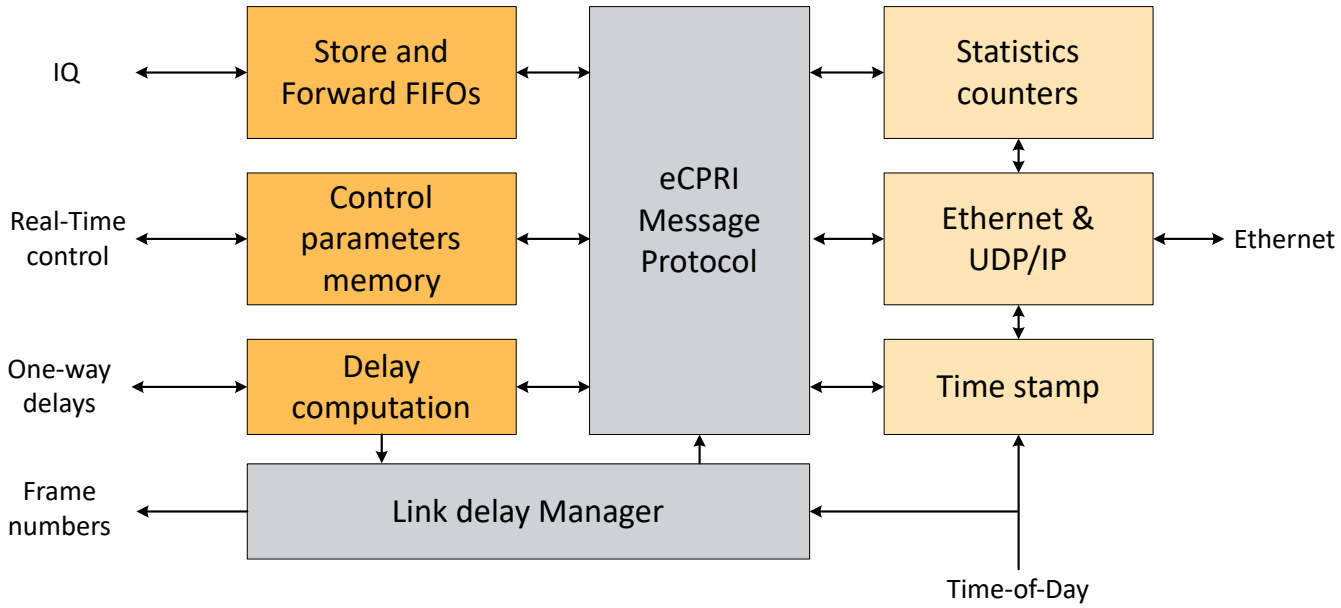
Overview

Chip Interfaces eCPRI core is a highly scalable and silicon agnostic implementation of the eCPRI standard targeting any ASIC, FPGA or ASSP technologies. The eCPRI implementation builds on long-time experience designing CPRI and Radio-Over-Ethernet solutions for fronthaul and delivers a flexible engine that is prepared for tight integration with software applications. The IP is designed to meet or exceed the requirements of radio systems, base band systems, fronthaul switches or advanced test systems. The speed optimized core can handle any solutions reaching from the "small footprint" to the most complex applications running 25 Gbps. The IP can dynamically be configured to handle wireless multi-mode radio systems enabling high-performance throughputs required by 4G and 5G wireless solutions.



Key Features

Richly Featured	Support for frequency-domain IQ transport Support for various functional split between RU and BBU Supports 10G/25G Ethernet MAC ports Agnostically supports multiple synchronization schemes Wide flexibility for configuring
Easy to use	Testbench with typical system configuration and examples
Silicon Agnostic	Designed in HDL and targeting any RTL implementation like ASICs, ASSPs and FPGAs
Highly Configurable	Supporting small to large system configurations

Specification

Feature	Availability	Default	Option	Comment
General Features				
Standard	eCPRI Specification V1.2	✓		
Functional Splits supported	eCPRI splits A to E / intra-PHY	✓		
Message Types Supported	0: IQ data	✓		
	1: Bit sequence	✓		
	2: Real-time control data	✓		
	3: Generic data transfer	✓		
	4: Remote memory access	✓		
	5: One-Way delay measurement	✓		
	6: Remote reset	✓		
	7: Event indication	✓		
Ethernet RX/TX traffic supported	10G and 25G	✓		
Support mandatory eCPRI EtherType	Yes	✓		
Support filtering of inbound Ethernet traffic based on MAC and packet headers	Yes		✓	
Supported protocol stacks	IPv4/IPv6 and UDP	✓		
VLAN tag insertion/removal	Yes	✓		
One-way delay measurement	1-step and 2-step		✓	
Support jumbo frames with up to 9000 bytes of MTU payload	Yes	✓		
Configurable size of receive buffering for UL/DL			✓	
Data (IQ) Interface	Avalon streaming	✓		
	AXI-S		✓	
Delay Measurement				
Support for external timing source	Yes	✓		
ToD input bus width	80 bits	✓		
Ethernet Interface				
Number of Ethernet ports towards network transport layer	1	✓		
Ethernet MAC interface standard	Avalon streaming	✓		
	AXI-S		✓	

Feature	Availability	Default	Option	Comment
CPU Interface				
Internal register width	32 bits	✓		
IRQ support	Yes	✓		
Interface standards supported	Avalon	✓		
	AXI4-Lite		✓	
	APB		✓	
Clock and Reset				
IP main clock frequency	Up to 390.625 MHz	✓		
IP CPU register clock frequency	100 MHz	✓		
IP Ethernet interface clock frequency towards Ethernet MAC	156.25/390.625	✓		10G/25G Ethernet support
Separate resets for RX, TX and Register interface	Yes	✓		
Deliverables				
Code	SystemVerilog	✓		Source code or Encrypted RTL
Documentation	Yes	✓		Including User Manual and Release Note
Simulation Environment	Yes	✓		Simple Test Environment, Test Cases and Test Scripts
Programming register specification	Yes	✓		
Timing Constraints in Synopsys SDC format	Yes		✓	
Access to Support System	Yes	✓		
Synopsys SGDC Files	Yes		✓	
Synopsys Lint, CDC and Waivers	Yes		✓	

Ordering Info

Delivery Option code	Delivery Option Code
B	RTL Source Code
C	Encrypted FPGA Netlist

Technology code	Target Technology
A	ASIC
F	FPGA

Model code	Model description
3	eCPRI